

TITLE OF THE INVENTION

DATA REPRODUCTION DEVICE

BACKGROUND OF THE INVENTION

5 FIELD OF THE INVENTION

The present invention relates to data reproduction devices for reproducing data recorded on memory cards, and more particularly to data reproduction devices which are designed to reduce power consumption.

~~10 BACKGROUND OF THE INVENTION~~

Sub
21 Digital audio players are conventionally known to read compressed audio data on various signal memory media and to expand and reproduce the audio data in the memory media. With the players, the data is recorded / reproduced at the bit rate of about 128 K bps, to produce fine quality sound. On the other hand, the development of the digital technology in recent years provides various data storage media. Attention is directed to one of the media, IC memory card which is adapted to write and read data at the high
15 bit rate, about a maximum of 8 Mbps.

Sub
22 Digital audio players having an IC memory card for use as a data storage medium are developed. In the digital audio players, data is written / read to IC memory card at the bit rate of about 128 Kbps in conformity with the bit

rate for decoding which is satisfactory in respect of sound quality. The power consumption of the IC memory card is generally constant during memory access regardless of the difference in the bit rate for data writing / reading.

5 *Sub 10* With the digital audio player having the IC memory card for use as the data storage medium, the use of a primary or a secondary battery as power source can realize its portability. However, the audio player of the portable type has the problem that the player is endurable to be used within the limited period of time since the primary or the secondary battery is limited in capacity.

SUMMARY OF THE INVENTION

10 *Sub 14* An object of the present invention is to provide a data reproduction device such as a digital audio player, etc. which has a memory card, and to prolong the period of time during which the player is endurable to be used by reducing its power consumption.

15 The present invention provides a data reproduction device comprising a control circuit for reading out data recorded on a memory card having a controller is mounted thereon, a data processing circuit for performing required processing to the read data and outputting the resulted data.

Sub 18 The controller of the memory card is so constructed

that an active mode is set wherein data is read out under current consumption in a first current value in response to memory access of data reading, and thereafter a standby mode automatically follows to wait for next memory access
 5 under current consumption in a second current value which is lower than in the first current value.

Further, the control circuit comprises a buffer for temporarily storing data read out from the memory card, a first control means for reading out data from the memory card at a first bit rate and storing the data, a second control means for reading out data stored in the buffer at a second bit rate which is lower than the first rate and supplying the data to the data processing circuit.

15 *Sub* With the data reproduction device of the invention, when a user manipulates to reproduce data, the control circuit repeats the operation to access to the memory card, and to read out intermittently predetermined amount of data from the memory card at the first bit rate. The read data is stored in the buffer.

20 In this operation, the controller of the memory card sets the active mode in response to the access from the control circuit to maintain the active mode until finishing reading out the predetermined amount of the data. In the active mode, the data is read out under the current

consumption in the first current value. When finishing reading out the predetermined amount of the data, the controller sets the standby mode after, for example, lapse of the predetermined period of time, and to wait for the
5 next memory access under the current consumption in the second current value.

The data stored in the buffer is read out at the second bit rate and supplied to the data processing circuit. This generates a given space area, causing the control
10 circuit to gain access to the memory card again and to start reading out the data from the memory card.

The data, as described above, is intermittently read out from the memory card, stored temporarily in the buffer, thereafter read out from the buffer at the low bit rate,
15 and supplied to the data processing circuit. This operation is repeated until all the data to be reproduced is read out from the memory card. Accordingly, either the active mode or the standby mode is alternatively set in the memory card, the current consumption in the standby mode is lower than
20 in the active mode. The current consumption in the active mode is constant regardless of the difference of the bit rate at the data reading.

Sub
at With the data reproduction device of the invention, as described, since power consumed by the memory card for

reading out all the data to be reproduced is a total value of the power consumption in the active mode and that in the standby mode, the power consumption is more reduced than in the conventional case where the memory card is always
5 accessed at the low bit rate which does not have a problem in data reproduction, to continue great current consumption.

BRIEF DESCRIPTION OF THE INVENTION

FIG. 1 is a block diagram showing the construction of a digital audio player embodying the invention;

FIG. 2 is a flow chart showing data reproduction control with the digital audio player; and

FIG. 3 is a time chart showing mode transition of a memory card.

DETAILED DESCRIPTION OF EMBODIMENT

15 *Sub*
12 A digital audio player embodying the present invention will be described below in detail with reference to the drawings. FIG. 1 shows that the digital audio player of the invention can be loaded with a memory card 8 having a controller 9 mounted thereon. The audio player comprises
20 a memory card controller 7 to control write / read of data to the memory card 8, a CPU 1 to execute various controlling operation like data reproducing in response to user's manipulation, a digital signal processing circuit DSP 3 to perform processing required for reproduction like

decoding, etc. on audio data read out from the memory card 8, a D/A converter 4 to convert digital audio signal obtained from the DSP 3 into analog audio signal, an amplifier 5 to amplify the audio signal obtained from the D/A converter 4 and to output the signal to a headphone 6. The CPU 1 has a buffer 2 incorporated therein, and is connected to a manipulating key 10 for a user giving the device a command for various operation.

The controller 9 mounted on the memory card 8, as shown in FIG. 3, sets an active mode A to read out data under the current consumption of 33mA in response to memory access of data reading. If there is no memory access within predetermined period of time T, a standby mode S automatically follows to wait for next memory access under the current consumption of $50 \mu A$.

In the embodiment, a power source voltage of the memory card 8 is set to 3V, a maximum bit rate is 8 Mbps at the data reading, and transition period of time T is 5 ms from the active mode to the standby mode.

FIG. 2 shows controlling procedure which the CPU 1 executes in data reproduction. An inquiry is made in step S1 as to whether PLAY key is turned on by user's manipulation. When PLAY key is on, the CPU 1 commands the memory card controller 7 to read the data from the memory

card 8 in step S2. This sets the memory card 8 in the active mode, to read the predetermined amount of data from the memory card 8 at the bit rate of 8 Mbps. When reading data access (active mode) from the memory card ends and the
 5 predetermined period of time T (=5 ms) elapses, the memory card 8 is into the standby mode.

The data read from the memory card 8 is temporarily stored in the buffer 2, and thereafter is read out from the buffer 2 at the bit rate of 128 Kbps. Subsequently, DSP 3 is given a command to start the reproduction operation in
 10 step S3.

Next in step S4, the CPU starts transferring data read out from the buffer 2 to the DSP 3. As a result, the data is given processing including decoding and the like
 15 required for reproduction by the DSP 3, and is D/A converted by the D/A converter to start the audio reproduction.

In step S5 the space of the buffer 2 is checked, and an inquiry is made in step S6 as to whether space area of
 20 the buffer is greater than the prescribed value. When the answer is No, step S4 follows again to continue the data transfer. This expands the space area of the buffer 2 gradually.

When the answer is Yes in step S6, step S7 follows.

In step S7 an inquiry is made as to whether the data to be read out is left on the memory card 8. When the answer is Yes, step S8 follows to re-read the predetermined amount of data from the memory card 8. Step S4, thereafter, follows again to continue the data transfer to the DSP 3.

On the other hand, when the answer is No, in step S7, Step S9 follows to give an inquiry as to whether all the data transfer is ended. When the answer is No, Step S4 follows again to repeat the data transfer. When the answer is Yes, the procedure ends.

The execution of the above procedure sets the active mode A or the standby mode S alternatively, to read out the data from the memory card 8 intermittently. This causes the data written on the buffer 2 of the CPU 1 to be read out successively, supplying the data to the DSP 3.

For example, in the case where the capacity of the buffer 2 of the CPU 1 is 16 Kbit, and the decoding bit rate of the audio data by the DSP 3 is 128 Kbps, as shown in FIG. 3, the data is reproduced by the repetition of data reading out period of 2 ms wherein the data is read from the memory card 8 in the active mode, transit period to the standby mode of 5 ms, and reading sleep period of 118 ms in the standby mode. The mean consumed current I is 1.9 mA calculated from the following Mathematical Expression 1.

(Mathematical Expression 1)

$$I = (2 \text{ ms} \times 33 \text{ mA} + 5 \text{ ms} \times 33 \text{ mA} + 118 \text{ ms} \times 50 \text{ } \mu\text{A}) / 125 \text{ ms}$$

$$= 1.9 \text{ mA}$$

5 *Sub* If data is successively read out from a memory card
all at the bit rate of 128 Kbps as conventionally in place of
 the intermittent reading method of the memory card
 according to the embodiment, the consumed current is 33 mA
 in constant, so that the power consumption is minimized to
 10 1 / 17 or less according to the invention. The increase of
 the capacity of the buffer 2 of the CPU 1 provides greater
 effect.

15 *Sub* The present invention described is particularly
all effective to the data reproduction device of the portable
 type since the intermittent data read out from the memory
 card enables the device to reduce the power consumption
 greatly.

20 The present invention is not limited to the foregoing
 embodiment in construction but can be modified variously by
 one skilled in the art without departing from the spirit of
 the invention as set forth in the appended claims. For
 example, the invention can be practiced not only for
 digital audio players but also for digital video devices
 such as digital cameras, etc.